



Application Notes

AN_376

Xilinx FPGA FIFO master Programming Guide

Version 1.0

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This document provides a guide on how to use Xilinx program tool iMPACT to program a Xilinx FPGA as a FIFO master for interfacing with UMFT600X/UMFT601X modules.

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1 Introduction

This document explains how to use Xilinx program tool iMPACT to program Xilinx FPGA as a FIFO master with the sample image for UMFT600X/UMFT601X module.

1.1 Overview

UMFT600X/UMFT601X modules are evaluation modules with FMC(LPC) high speed connectors, providing a USB3.0 to 16Bit/32Bit wide parallel FIFO interface, which are used to evaluate the functionality of FT600/FT601 devices.

As a FIFO slave board, the UMFT600X/UMFT601X operates with a FIFO master board which has a standard FMC connector. This document explains how to program a Xilinx FPGA(Spartan-6 FPGA SP601 Evaluation Kit and Virtex-6 LX240T Evaluation Kit) as a FIFO master with the sample image, so that user can run '[FT600DataLoopbackApp](#)' to verify module's functions.

1.2 Prerequisite

- A PC with Xilinx program tool iMPACT (Assume Xilinx drivers have been installed.)
- Xilinx Spartan-6 FPGA SP601 evaluation Kit
- Xilinx Virtex-6 LX240T FPGA HTG-V6-PCIE Evaluation Kit and Platform Cable USB II

1.3 Notes

FTDI provides 8 different FPGA loopback application images and 2 PCB evaluation boards with an HSMC connector that is compatible with xilinx FPGA development kits. Ensure the FPGA image used, matches with the PCB evaluation board i.e. UMFT600 or UMFT601 and either 600 mode or 245 mode of operation. Data transfer will not work properly if the FPGA image is incompatible with the PCB evaluation board.

FPGA loopback application images

- Xilinx FPGA-Spartan-6 SP601, FT601, 600 mode
- Xilinx FPGA-Spartan-6 SP601, FT601, 245 mode
- Xilinx FPGA-Virtex-6 HTG-V6-PCIE, FT601, 600 mode
- Xilinx FPGA-Virtex-6 HTG-V6-PCIE, FT601, 245 mode
- Xilinx FPGA-Spartan-6 SP601, FT600, 600 mode
- Xilinx FPGA-Spartan-6 SP601, FT600, 245 mode
- Xilinx FPGA-Virtex-6 HTG-V6-PCIE, FT600, 600 mode
- Xilinx FPGA-Virtex-6 HTG-V6-PCIE, FT600, 245 mode

PCB evaluation boards

- UMFT601X (HW_433) – For Xilinx FPGA with FT601 image
- UMFT600X (HW_431) – For Xilinx FPGA with FT600 image

2 Step-by-step instruction

2.1.1 Spartan-6 SP601

1. Connect the SP601 J10 (USB JTAG) to a PC with a mini-USB cable,
2. Apply DC5V to J18, then turn on the POWER (SW1 to ON.)
3. On the SP601 all SW and Jumpers are configured as default:

SW2-SPI Flash	J4-Exclude FMC	SW8
1-on 2-off	Short 1-2	1-off 2-on 3-off 4-off

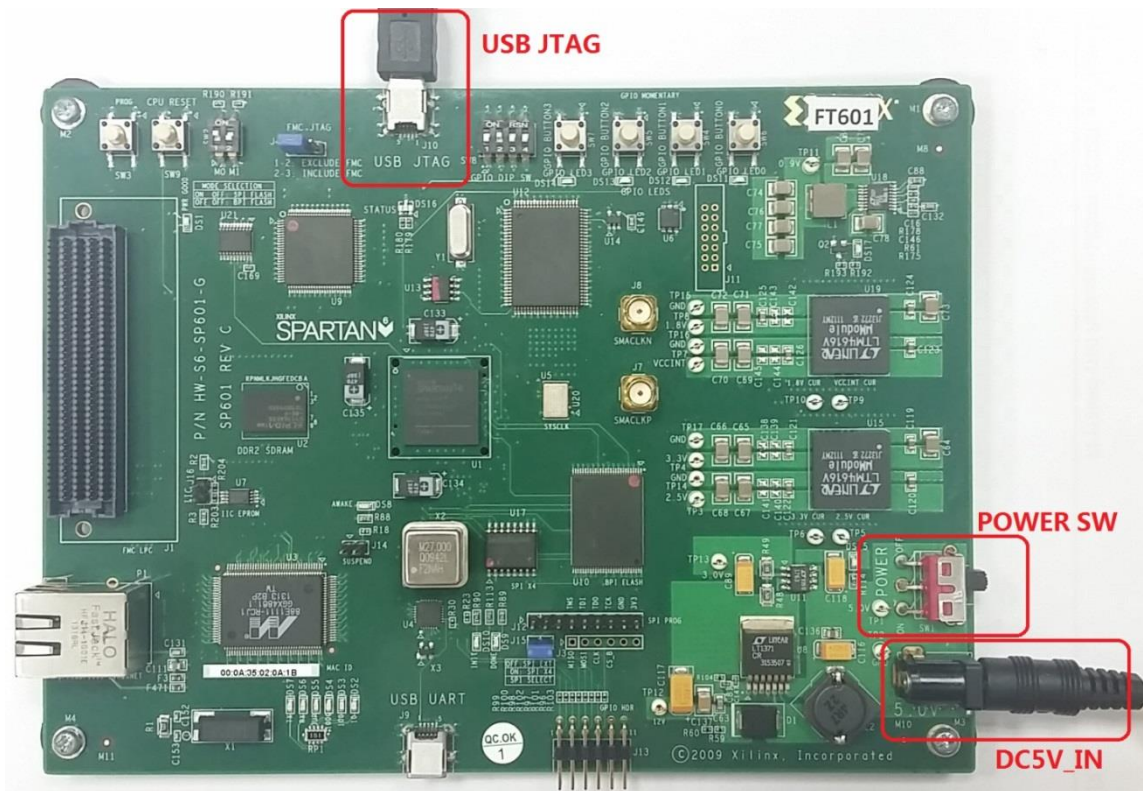


Figure 2.1 SP601 Hardware Setup

- Run the Xilinx program tool iMPACT, the New iMPACT Project interface will appear, then click 'Cancel' to return to the main interface.

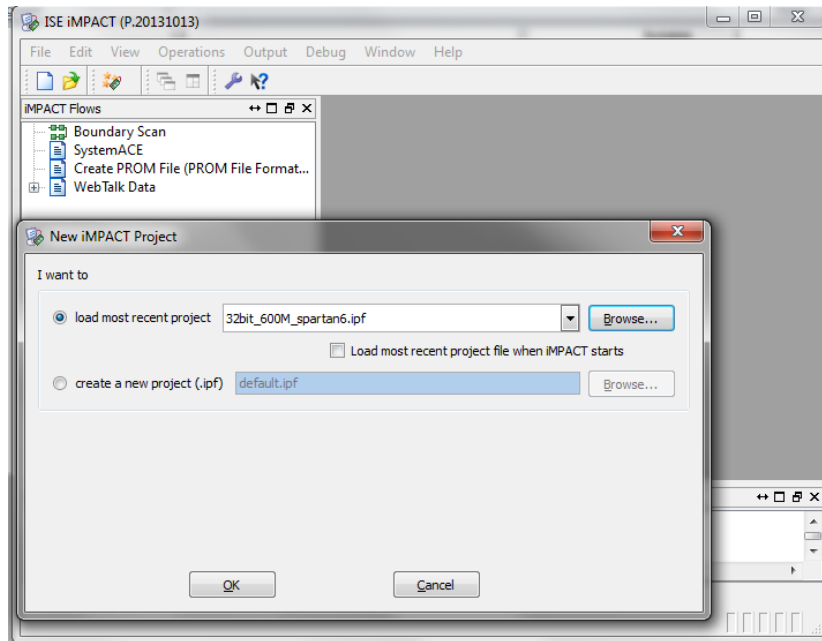


Figure 2.2 iMPACT User Interface

- Double click 'Boundary Scan' at the iMPACT Flows window.
- Move the mouse pointer to the right side window and right click, select 'Initialize Chain'.
- The tool will search and find the JTAG device automatically.

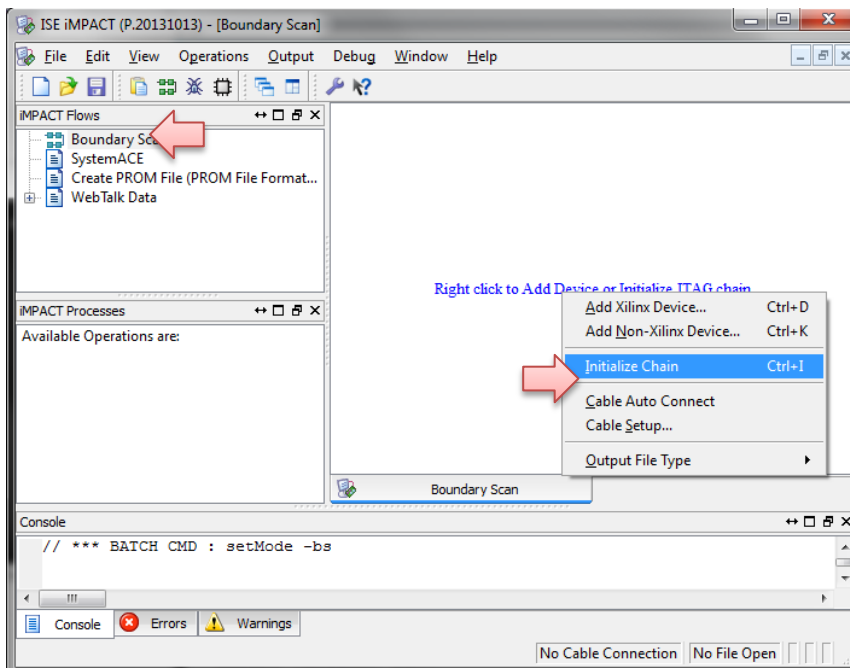


Figure 2.3 Boundary Scan and Initialize Chain

8. If iMPACT found the device, click 'Yes' to assign the demo FPGA configuration file and specify the sample bit file for the FPGA.

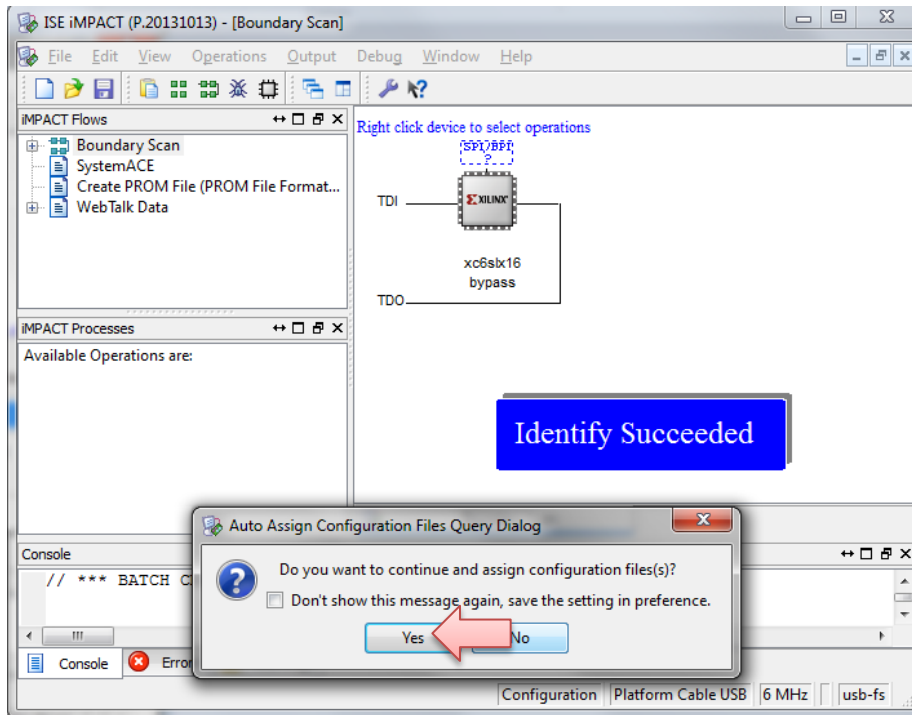


Figure 2.4 Found Device

9. The selected bit file will be shown in the device window.
10. The Flash PROMs interface will now appear.
11. Click 'Yes' to program SPI flash or click 'No' to skip and program the FPGA only.

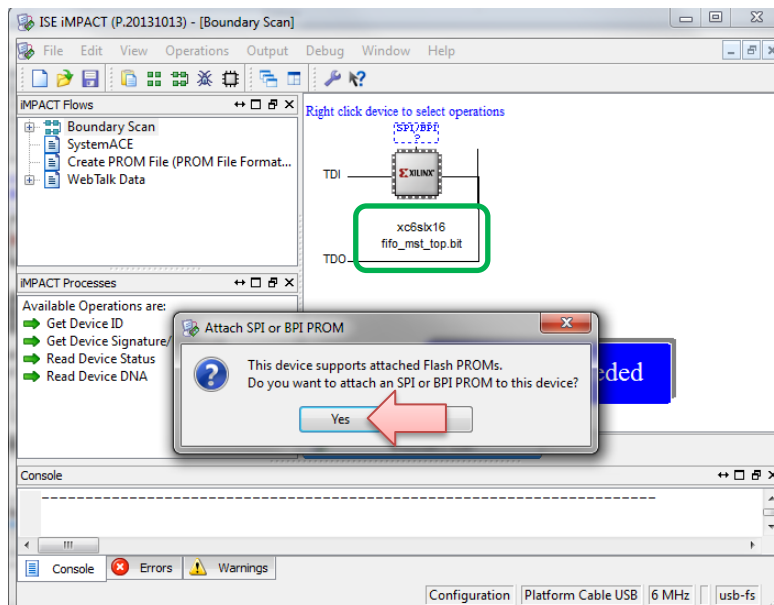


Figure 2.5 Assign FPGA configure file successfully

12. After specifying the .mcs files the interface shown below will appear,
13. Select "SPI PROM" and Flash select "W25Q64FV", data width select '1'.

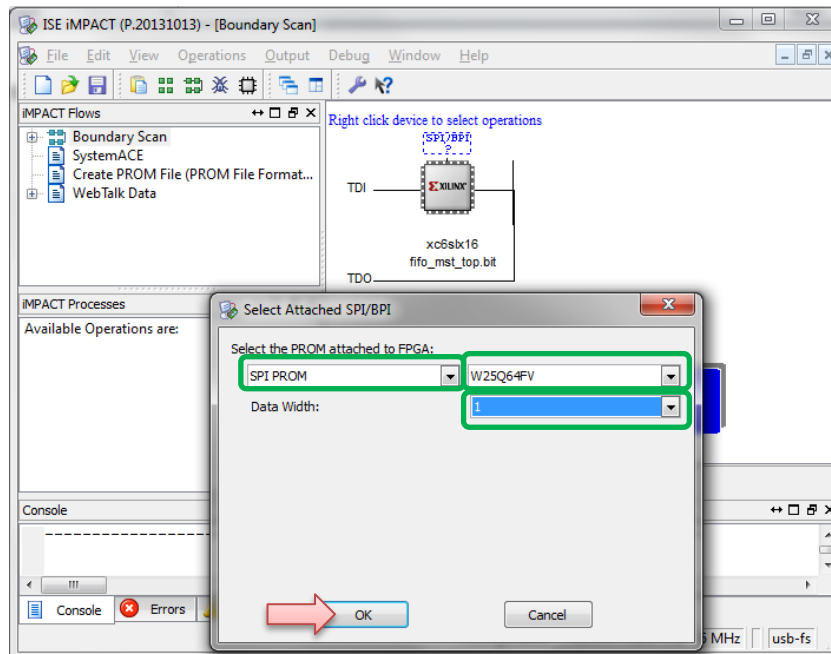
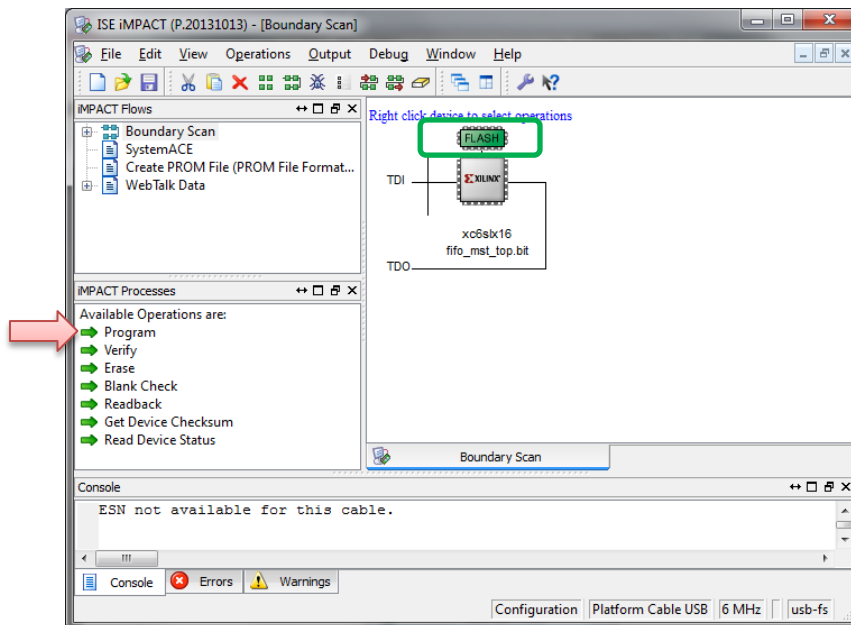


Figure 2.6 Assigning File for Flash and select flash type

14. Select 'FLASH' or 'Xilinx' FPGA device then double click 'Program' for programming SPI flash or FPGA.



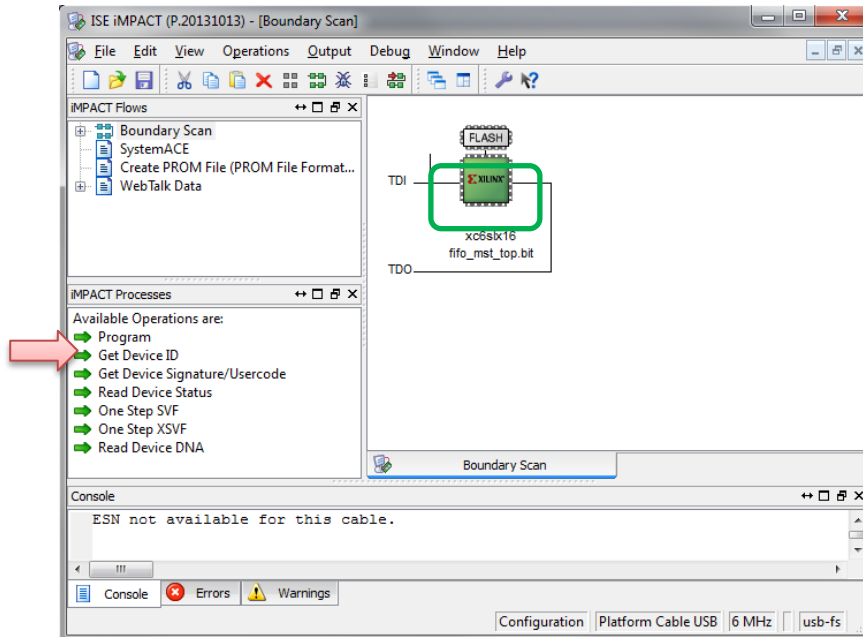
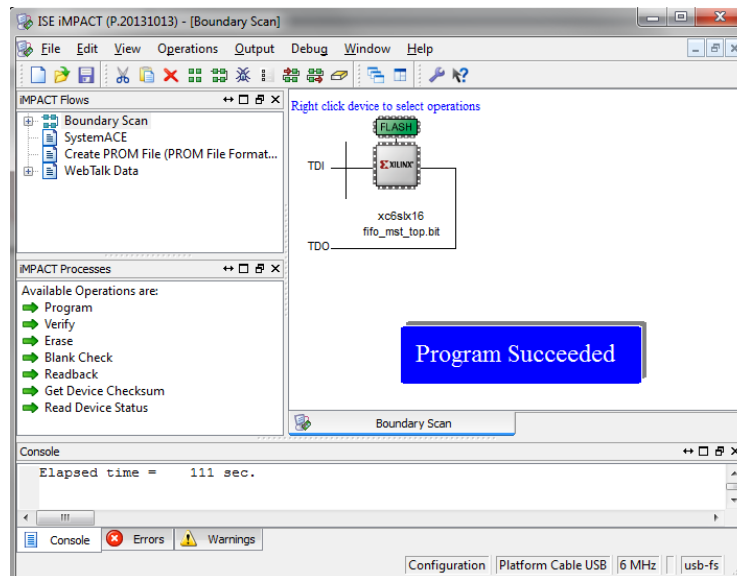


Figure 2.7 Select Program Device

15. Information message 'Program Succeeded' will be shown after programming successfully.



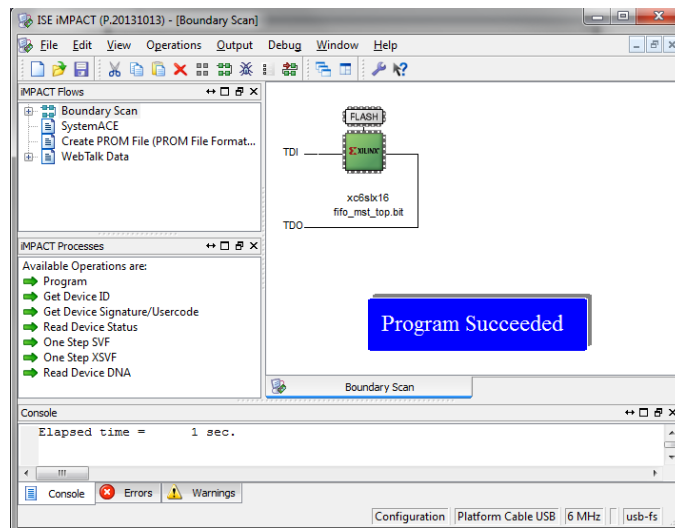


Figure 2.8 Program Successfully

2.1.2 Virtex-6 LX24T HTG-V6-PCIE

1. Connect the "Platform Cable USB II" to the HTG-V6-PCIE J35 (JTAG) with the JTAG cable, and connect to a PC with a USB2.0 cable. Plug in DC12V to J11, and then turn on POWER (SW11). The HTG-V6-PCIE uses default setting.

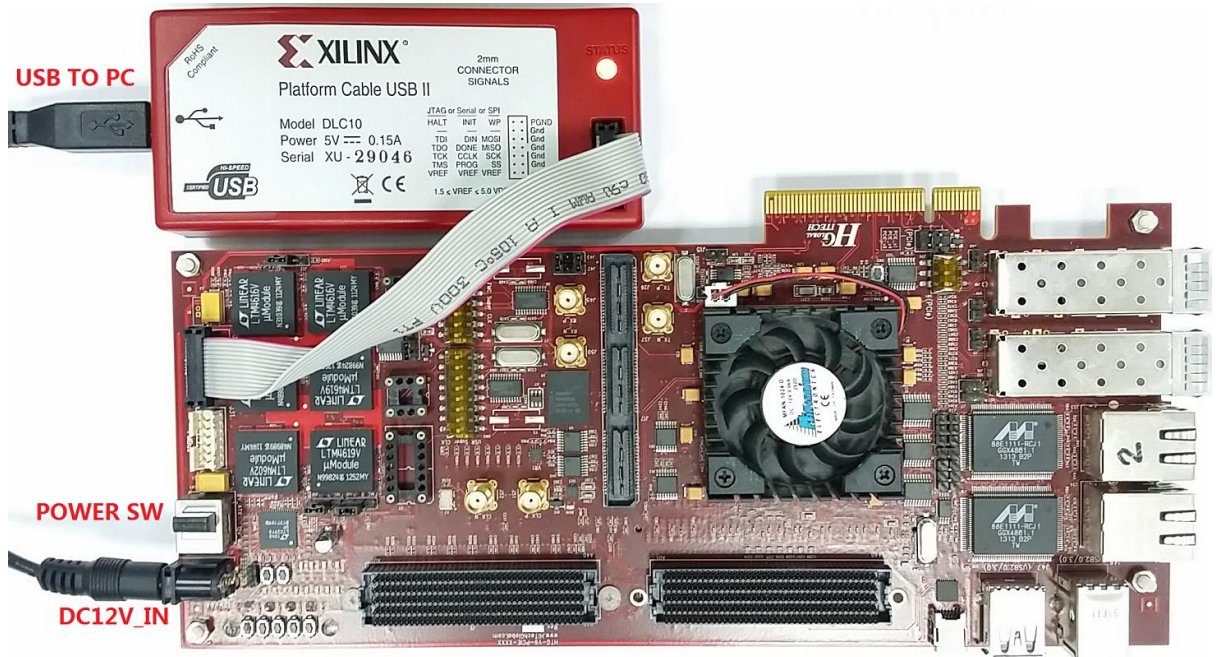
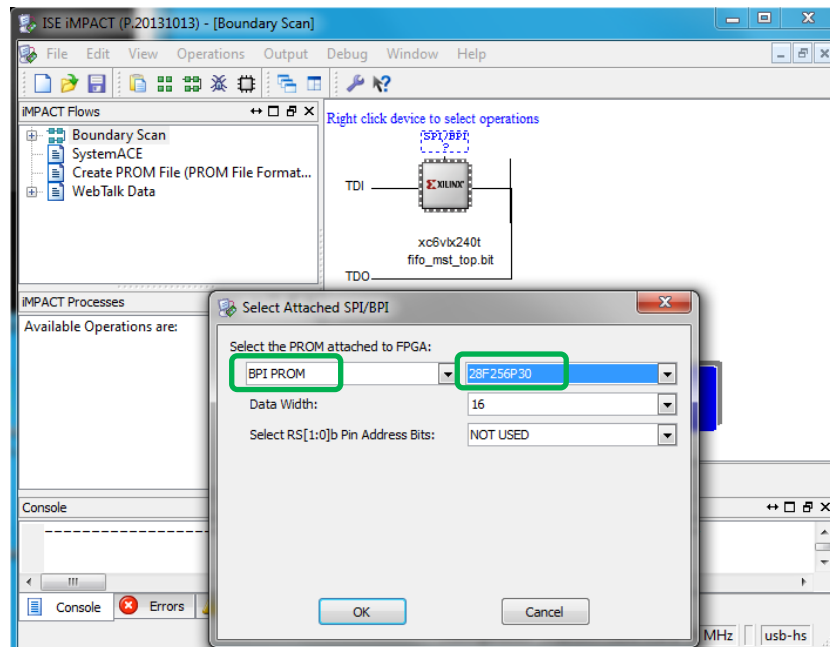


Figure 2.9 HTG-V6-PCIE Hardware Setup

- The procedures of programming FPGA LX240T or Flash are same as section [2.1.1](#), but the files for FPGA and Flash are different, the Flash type is 'BPI', and the flash model is '28F256P30', with a data width of 16.

**Figure 2.10 HTG-V6-PCIE Flash Selection**

3 UMFT600X/UMFT601X Data Loopback Demo

1. Hardware setup: Plug the UMFT600X or UMFT601X module into the SP601 or HTG-V6-PCIE board; connect the UMFT600X or UMFT601X CN1 to the PC with a micro-USB3.0 cable. Plug in a DC supply to the SP601 or HTG-V6-PCIE board, and then turn on the POWER.

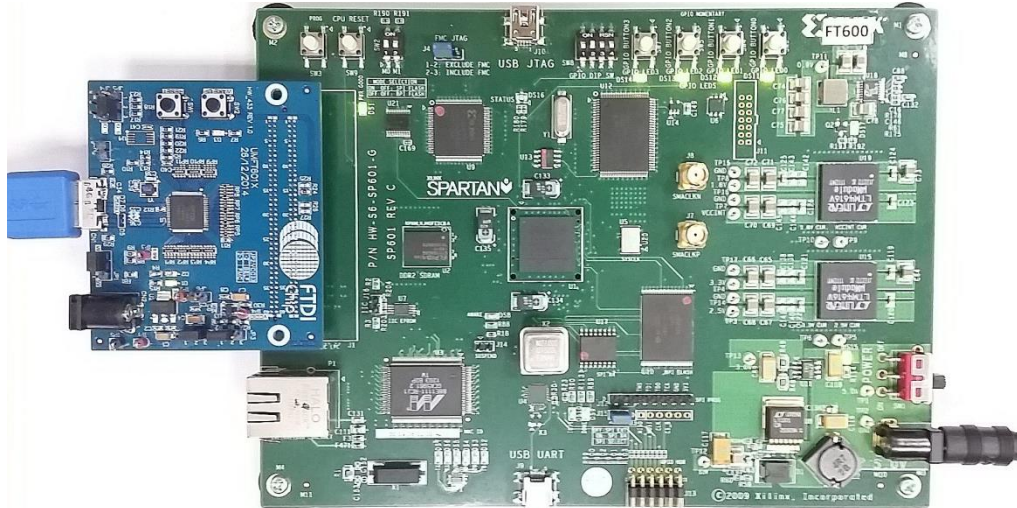


Figure 3.1 UMFT600X/UMFT601X + SP601 data loopback demo hardware setup

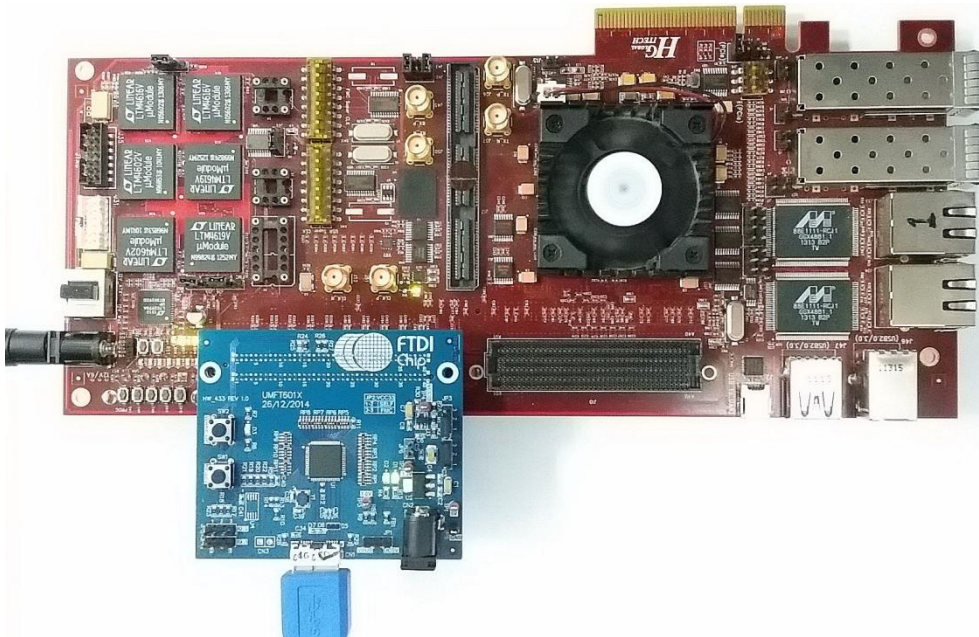


Figure 3.2 UMFT600X/UMFT601X + HTG-V6-PCIE data loopback demo hardware setup

- Run the 'FT600DataLoopbackApp', the application will find the device automatically; click the 'Start All' button to do an all channels data loopback test. Refer to 'AN_375 FT600 Data Loopback Application User Guide' for more details of this application.

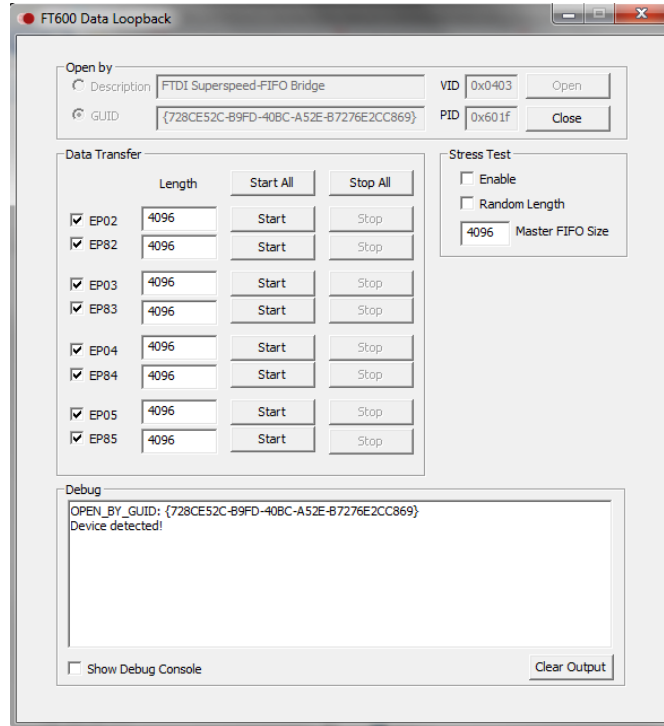


Figure 3.3 FT600 Data Loopback application

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Appendix A – Document References

[FT600Q-FT601Q SuperSpeed USB3.0 IC Datasheet](#)

[AN_375 FT600 Data Loopback Application User Guide](#)

[DS_UMFT60xx module datasheet](#)

[D3XX Programmer's Guide](#)

[AN_385 D3xx Installation Guide](#)

[Xilinx Firmware Download](#)

[Loopback utility](#)

Getting Started with the Spartan-6 FPGA SP601 Evaluation Kit User Guide
http://www.xilinx.com/support/documentation/boards_and_kits/ug523.pdf

SP601 Hardware User Guide
http://www.xilinx.com/support/documentation/boards_and_kits/ug518.pdf

SP601 Hardware Setup Guide
http://www.xilinx.com/support/documentation/boards_and_kits/xtp049.pdf

HTG-V6-PCIE FPGA evaluation kit Hardware Setup Guide
http://www.hitechglobal.com/Boards/Virtex6_PCIExpress_Board.htm

Appendix B – Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out
FMC	Field Programmable Mezzanine Card
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group
LPC	Low Pin Count
USB	Universal Serial Bus

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Appendix D – Revision History

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